

### AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device comprising:  
  
a semiconductor chip diced from a semiconductor substrate with a prescribed element and an electrode portion formed on its main face and having ~~without removing~~ a conductive film ~~from~~ on a dicing line region;  
  
a conductive wire connected to said electrode portion; and  
  
an insulating sheet member for covering part of said conductive film along periphery of said semiconductor chip.
  
2. (Original) The semiconductor device according to claim 1, wherein  
  
said insulating sheet member is provided for covering a back face of said semiconductor chip, a side face of said semiconductor chip, and part of the front face along periphery of said semiconductor chip.
  
3. (Original) The semiconductor device according to claim 2 comprising a plurality of  
  
said semiconductor chips covered by said insulating sheet member, wherein said plurality of semiconductor chips are layered.
  
4. (Original) The semiconductor device according to claim 1, wherein said insulating sheet member is provided for covering the front face of said semiconductor chip and a side face of said semiconductor chip.

5. (Original) The semiconductor device according to claim 4 further comprising an opening formed in said insulating sheet member at a position corresponding to said electrode portion, wherein said conductive wire is connected to said electrode portion through said opening.

6. (Original) The semiconductor device according to claim 5 comprising a plurality of said semiconductor chips covered by said insulating sheet member, wherein said plurality of semiconductor chips are layered.

7. (Original) The semiconductor device according to claim 4 comprising a plurality of said semiconductor chips covered by said insulating sheet member, wherein said plurality of semiconductor chips are layered.

8. (Original) The semiconductor device according to claim 1 comprising a plurality of said semiconductor chips covered by said insulating sheet member, wherein said plurality of semiconductor chips are layered.